

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	192	703/28.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/13 11:24
L2	2649	(variable or adjustable) near clock	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 11:32
L3	2588	L2 and @ad<"200100510"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 11:34
L4	2	(dynamically adj programmable) near clock	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 11:34
L5	1925	programmable near clock	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 11:34
L6	1902	L5 and @ad<"200100510"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 12:32
L7	250	L6 and (fpga or pld)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 12:32
L8	217	dynamic adj clock	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/13 12:32
L9	211	L8 and @ad<"200100510"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 12:33
L10	145	L8 and @ad<"20010510"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/13 12:33



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Select Article Information

- ☐ 1. **Dynamic clock management for low power applications in FPGAs**
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- ☐ 2. **Asynchronous processor survey**
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 Volume 30, Issue 11, Nov. 1997 Page(s):67 - 76
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[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(352 KB) IEEE JNL
- ☐ 3. **Router plugins: a software architecture for next-generation routers**
 Decasper, D.; Dittia, Z.; Parulkar, G.; Plattner, B.;
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 Volume 8, Issue 1, Feb. 2000 Page(s):2 - 15
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